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ORIGINALLY FILED

Attorney Docket DA01028/1346P

GP 2811

CERTIFICATE OF MAIL

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on December 19, 2001.

Joseph A. Sawyer, Jr.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:

Date: December 19, 2001

Mark S. CHANG et al.

Serial No.: 09/539,458

Group Art Unit: 2814

Filed: March 30, 2000

Examiner: Pham, H.

For: METHOD AND SYSTEM FOR PROVIDING CONTACT TO A FIRST
POLYSILICON LAYER IN A FLASH MEMORY DEVICE

Assistant Commissioner for Patents
Washington, D.C. 20231

TRANSMITTAL LETTER

Sir:

In response to the Office Action dated September 25, 2001, please find enclosed the following:

- 1) Transmittal Letter (original and one copy)
- 2) Amendment responsive to the Office Action dated September 25, 2001
- 3) Postcard
- 4) The fee for claims has been calculated as shown below:

<input checked="" type="checkbox"/> Large Entity		<input type="checkbox"/> Small Entity			
Fee Items	Claims remaining after Amendment	Highest # of Claims previously paid for	Extra Claims	Fee Rate	TOTAL
Total Claims	16	- 20 =	0	x 18	\$ 0.00
Independent	2	- 3 =	0	x 84	\$ 0.00
Multiple Dependent Claim fee (one or more, first added by this amendment)				280.00	\$ 0.00
Total Fees					\$ 0.00

If any unresolved issues remain, please contact Applicant's attorney at the telephone number below. The Commissioner is hereby authorized to charge any fees associated with this communication, or credit any overpayment, to Deposit Account No. 01-0365 (Advanced Micro Devices, Inc).

Respectfully submitted,

December 19, 2001

Date

Joseph A. Sawyer, Jr.
Attorney for Applicants
Reg. No. 30,801
(650) 493-4540



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Assistant Commissioner of Patents
Washington, D.C. 20231

AMENDMENT

Sir:

In response to the Office Action dated September 25, 2001, please amend the above-identified application in the following manner:

CLAIMS

1. (Amended) A flash memory device comprising:
- a plurality of gate stacks including a plurality of floating gates and a plurality of control gates disposed on a semiconductor substrate;
 - at least one component including a polysilicon layer having a top surface;
 - a silicide on the top surface of the polysilicon layer of the at least one component;